

Claims

1. A data processing architecture comprising:  
an input device for receiving an incoming stream of  
data packets; and  
5 a plurality of processing elements which are operable  
to process data received thereby;  
wherein the input device is operable to distribute data  
packets in whole or in part to the processing elements in  
dependence upon the data processing bandwidth of the  
10 processing elements.
2. A data processing architecture as claimed in claim 1,  
wherein the processing elements are arranged in a single  
instruction multiple data (SIMD) array.  
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3. A data processing architecture as claimed in claim 1,  
wherein a data packet is allocated to a plurality of  
processing elements.
- 20 4. A data processing architecture as claimed in claim 1,  
wherein the input device is operable to divide the incoming  
data packet stream into processor data packets of a fixed  
size for distribution to the processing elements.
- 25 5. A data processing architecture as claimed in claim 4,  
wherein the input device is operable to distribute whole or  
part of a data packet to a processing element.
6. A data processing architecture as claimed in  
30 claim 1, wherein the input device is operable to  
transfer data packets to the processing elements such that  
not all processing elements receive data.

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7. A data processing architecture as claimed in claim 1, wherein the processing elements are operable to control the input device.

5 8. A data processing architecture as claimed in claim 7, wherein the processing elements are operable to control the input device by means of software.

9. A data processing architecture as claimed in claim 1,  
10 wherein the processing elements are operable to control an output device.

10. A data processing architecture comprising:  
an input/output system which is operable to receive an  
15 incoming stream of data packets; and  
a plurality of processing elements operable to receive data from, and transmit data to, the input/output system,  
wherein the input/output system is operable to divide  
the incoming stream of data packets into a stream of  
20 processor data packets of a fixed size, to distribute processor data packets to the processing elements, to collect processor data packets from the processing elements and to construct an outgoing data packet stream from collected processor data packets.

25 11. A data processing architecture as claimed in claim 10, comprising a plurality of such input/output systems, which support multiple input/output operations.

30 12. A single instruction multiple data (SIMD) data processing architecture comprising:  
a plurality of processing elements which are operable to receive data and to process that data,

wherein at least one processing element is operable to enter a standby mode of operation in dependence upon data received by that processing element.

5 13. An architecture as claimed in claim 12, wherein the at least one processing element is operable to enter the standby mode of operation when no data is received.

14. A data processing architecture comprising:

10 a parallel array of processing elements arranged in a single instruction multiple data processing array;  
a hardware accelerator unit operable to receive, in series, processing requests from the processing elements and to return processing results to respective processing  
15 elements when those processing results are available; and

an input/output system which is operable to transfer respective processing requests from the processing elements to the hardware accelerator, and to return processing results to the processing elements concerned,

20 wherein the processing elements are operable to process the returned processing results when all such results are returned, or after a predetermined time period.

15. A data processing architecture comprising:

25 a parallel array of processing elements arranged in a single instruction multiple data processing array;

a hardware accelerator unit operable to receive, in series, processing requests from the processing elements and to return processing results to respective processing

30 elements in the order in which processing requests were received by the accelerator unit; and

an input/output system which is operable to transfer respective processing requests from the processing elements

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to the hardware accelerator, and to return processing results to the processing elements concerned,

wherein the processing elements are operable to process the returned processing results when all such results are  
5 returned, or after a predetermined time period.

16. A data processing architecture as claimed in claim 14,  
comprising a first plurality of parallel arrays of  
processing elements, and a second plurality of hardware  
10 accelerator units.

17. A data processing architecture comprising a plurality  
of parallel arrays of processing elements, and a data I/O  
structure which is operable to transfer data to and from the  
15 arrays of processing elements in turn.

18. A data processing architecture comprising a plurality  
of processing elements arranged in a SIMD processing array,  
wherein a plurality of processing elements are arranged for  
20 processing a single input data packet.

19. An architecture as claimed in claim 1,  
wherein each processing element is operable to  
process data stored by that element in accordance with  
25 processing steps determined by the data concerned.

20. An architecture as claimed in claim 1,  
comprising a plurality of functional blocks chosen from: a  
SIMD processing element array, a data input device, a data  
30 output device, a hardware accelerator, a data packet buffer  
and a bus structure for connecting the functional blocks to  
one another.

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21. An architecture as claimed in claim 1,  
implemented on a single integrated circuit.

5 22. An architecture as claimed in claim 1,  
implemented on a plurality of integrated circuits.

23. An input/output system for transferring data to and  
from a plurality of processing elements arranged in a single  
10 instruction multiple data (SIMD) array, the system being  
operable to transfer data packets of different sizes to  
respective ones of the processing elements in the array.

24. A system as claimed in claim 23, operable to transfer  
15 the data packets to respective different addresses in the  
processing elements.

25. A system as claimed in claim 23, wherein data  
packet transfer is controlled by the processing elements in  
20 the array.

26. A system as claimed in claim 23, operable to transfer  
the data packets to the processing elements when a batch of  
data packets are ready for transfer in an input device.  
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27. A system as claimed in claim 23, operable to transfer  
the data packets to the processing elements when part of a  
batch of data packets are ready for transfer in an input  
device.

30 28. A system as claimed in claim 27, wherein the part batch  
is transferred in response to a request from the processing  
elements.

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29. A system as claimed in claim 23, operable to transfer data packets from the processing elements to an output device when a full batch has been processed.

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30. A system as claimed in claim 23, operable to transfer data packets from the processing elements to an output device when part of batch has been processed.

10 31. A system as claimed in claim 26, wherein the decision to transfer full or part batches is made in dependence upon the speed of the processing elements and the speed and intermittency of the data packets.

15 32. A processor comprising an architecture or system as claimed in claim 1.

33. A data processing architecture as claimed in claim 15, comprising a first plurality of parallel arrays of processing elements, and a second plurality of hardware accelerator units.

34. An architecture as claimed in claim 10, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

35. An architecture as claimed in claim 12, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

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36. An architecture as claimed in claim 14, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

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37. An architecture as claimed in claim 15, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

38. An architecture as claimed in claim 17, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

39. An architecture as claimed in claim 18, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

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40. An architecture as claimed in claim 10, implemented on a single integrated circuit.

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41. An architecture as claimed in claim 12, implemented on a single integrated circuit.

42. An architecture as claimed in claim 14, implemented on a single integrated circuit.

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43. An architecture as claimed in claim 15, implemented on a single integrated circuit.

44. An architecture as claimed in claim 17, implemented on a single integrated circuit.

45. An architecture as claimed in claim 18, implemented on a single integrated circuit.

46. An architecture as claimed in claim 10, implemented on a plurality of integrated circuit.

47. An architecture as claimed in claim 12, implemented on a plurality of integrated circuit.

48. An architecture as claimed in claim 14, implemented on a plurality of integrated circuit.

49. An architecture as claimed in claim 15, implemented on a plurality of integrated circuit.

50. An architecture as claimed in claim 17, implemented on a plurality of integrated circuit.

51. An architecture as claimed in claim 18, implemented on a plurality of integrated circuit.

52. A processor comprising an architecture or system as claimed in claim 10.

53. A processor comprising an architecture or system as claimed in claim 12.

54. A processor comprising an architecture or system as claimed in claim 14.



55. A processor comprising an architecture or system as  
claimed in claim 15.

56. A processor comprising an architecture or system as  
5 claimed in claim 17.

57. A processor comprising an architecture or system as  
claimed in claim 18.

58. A processor comprising an architecture or system as  
claimed in claim 23.

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